URN etd-0407109-183720-1634
Author Su-Wei Tsai
Author's Email Address No Public.
Statistics This thesis had been viewed 75 times. Download 243 times.
Department
Year 2005
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Design and Implementation of Motion Image Detection for Embedded System
Date of Defense 0000-00-00
Page Count 103

Keyword
FPGA
SoPC
Motion detection
Image Processing

Abstract
Image motion detection is a fundamental part of machine vision related research projects. It applies for vehicle speed estimation, target tracking and recognition, etc. In this study, the captured image will be analyzed for moving object and estimation of its moving path and speed. The results are useful for developing an intelligent surveillance system with automatic tracking capability.
In this work, the entire system was developed using the software/hardware co-design methodology, which includes the camera interface, VGA interface, embedded Nios II CPU, image processing, and the operating system -- MicroC/OS-II. The camera interface consists of camera control circuit, image buffer, RGB to YCbCr converter, and DMA controller, which stores the image data from the buffer into an external SDRAM. The VGA interface consists of YCbCr to RGB converter, two output buffers, VGA controller and DMA controller, which gets the processed image data from the SDRAM and writes into the first buffer; while the VGA controller outputs the image from the second buffer. The algorithm of motion image detection is processed by the embedded Nios II CPU, by subtract the current image captured through the CMOS camera with the pre-recorded background first, and processes then the object detection for the remaining image. As a result of this procedure, if any motion part in the scene was founded, the centre position of the moving target will be marked, and its moving path and speed can be calculated.
The design and implementation of this embedded image processing system for motion detection is based on an Altera DE2 development board using highly integrated SOPC builder. The experiment result shows this system can fulfill the demand of compact size, and low cost.
Advisory Committee Chao-Huang Wei - advisor

Files etd-0407109-183720-1634-002.pdf
etd-0407109-183720-1634-001.pdf

indicate access worldwide
Date of Submission 2006-08-17